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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,559	IWATA, YOSHIHISA	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-14 and 16-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-14,23 and 24* is/are allowed.

6)☒ Claim(s) *16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 22 is objected as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear what applicant refers to as an external input signal in claim 12, line 10, because it is not shown in the drawing. Only the recited input signal Vin is shown in Fig. 7. Please direct to the drawing for clarification.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 16, 21 and 22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The first and second reference signals are inputted from outside of the semiconductor apparatus was not described or mentioned in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 22 is rejected under 35 U.S.C. 102(e) as being anticipated by Marr (US 2004/0199841).

In claim 22, Marr teaches all claimed features in Fig. 2A and 3, a semiconductor apparatus having a logic level decision circuit (Fig. 2A), the logic level decision circuit comprising: a first comparison circuit (222) which compares an input signal (SIN) with a first reference signal (VREF1) corresponding to logic "1" level, and which outputs a first differential signal (210); a second comparison circuit (224) which compares the input signal (SIN) with a second reference signal (VREF2) corresponding to logic "0" level, and which outputs a second differential signal (212); and a third comparison circuit (202) which compares output of the first comparison circuit and output of the second comparison circuit, and which decides a logic level (SOUT) of the input signal.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 16-18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA) in Fig. 1 in view of Marr (US 2004/0199841).

In claim 16, the AAPA in Fig. 1 teaches a signal transmission system which transmits and receives binary logic signals (logic 1 and logic 0) between a plurality of semiconductor apparatuses (100s), wherein the plurality of semiconductor apparatuses respectively have an input receiver (101 in Fig. 1 of AAPA) that decides a logic level of an external input signal (Vin); with the exception of teaching a first and a second reference voltages. However, Marr teaches in Figs 2A and 3, a first reference signal (VREF1) corresponding to a logic "1" level of the input signal and a second reference signal (VREF2) corresponding to a logic "0" level are supplied as reference signals for logic level decision to the respective input receivers.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of the AAPA in Figs 1 and 2 with the teachings of Marr in order to provide mode detection circuits that can be used for transmitting signals in semiconductor circuits such as memory devices that allow user to switch between test mode and operation mode.

In claim 17, Marr teaches all claimed features the signal transmission system of claim 16; with the exception of teaching wherein the plurality of semiconductor apparatuses are packaged on a same wiring board, and structure a semiconductor module. However, the AAPA in fig. 1 teaches the plurality of semiconductor apparatuses (100s) are packaged on a same wiring board (Fig. 1), and structure a semiconductor module (as seen in Fig. 1).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to combine the teaching of Marr and the AAPA in Fig. 1 in order to provide a plurality of semiconductor apparatuses for the signal transmission system.

In claim 18, Marr further teaches the signal transmission system of claim 16, wherein each of the input receivers including: a first comparison circuit (222) which compares an input signal (SIN) with a first reference signal (VREF1) corresponding to logic "1" level, and which outputs a first differential signal (210); a second comparison circuit (224) which compares the input signal (SIN) with a second reference signal (VREF2) corresponding to logic "0" level, and which outputs a second differential signal (212); and a third comparison circuit (202) which compares output of the first comparison circuit and output of the second comparison circuit, and which decides a logic level (SOUT) of the input signal.

Claim 21 corresponds to detailed circuitry already discussed similarly with regard to claim 16.

8. Claims 19 and 20 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

9. Claims 9-14, 23 and 24 appear to comprise allowable subject matter of the first comparison circuit is a current mirror type first voltage comparison circuit, and the second comparison circuit is a current mirror type second voltage comparison circuit.

Response to Arguments

10. Applicant's arguments with respect to claims 16, 21 and 22 have been considered but are moot in view of the new ground(s) of rejection.

The new grounds of rejection have been set as discussed in detailed action above.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VIBOL TAN
PRIMARY EXAMINER